REMARKS/ARGUMENTS

Claims 16 through 30 are pending in this application. The Abstract has been replaced and a clean copy is attached herewith.

The Office Action asserts that the preliminary amendment was unclear as to which claims were cancelled and for purposes of the examination claims 2, 6, 12 and 13 were considered cancelled. Applicant asserts that these claims were not cancelled. In order to clarify the pending claims, applicant has cancelled claims 1 through 15 and submitted claims 16 through 30. Newly added claims 16 through 30 are representative of the claims that were intended to be prosecuted and this amendment is not being made for purposes of patentability.

The Office Action objects to the form of the Abstract. A replacement abstract has been provided.

The Office Action rejects claims 8-11 and 14-15 under 35 U.S.C. §112, second paragraph, contending that these claims fail to particularly point out and distinctly claim the subject matter. This rejection is moot as to claims 8-11 and 14-15, which have been cancelled. Applicant submits that claims 16 through 30 particularly point out and distinctly claim the subject matter of the invention and that this rejection should be withdrawn. In particular, claims 23 and 26 clarify the means for implementing the column interleaving function.

The Office Action rejects claims 1, 3-5, 7-10 and 14 under 35 U.S.C. §102(a) as being anticipated by U.S. Patent No. 6,625,763 to Boner. This rejection is moot as to claims 1, 3-5, 7-10 and 14, which have been cancelled.

With respect to claims 16 through 30, applicant respectfully submits that Boner fails to disclose or suggest the feature of these claims of providing a number of memories equal to the maximum number of columns in the interleaving function.

Boner discloses a block interleaver 300 comprising a relatively small register file 301 and

a single larger random access memory 200 as shown in Figure 3:

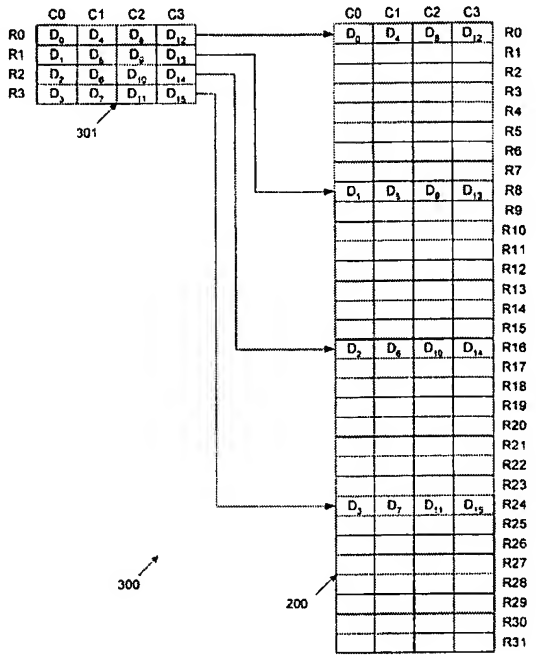

FIG. 3

Boner makes clear that RAM 200 is to be a single memory device:

> After register file 301 has been filled, the 4-bit values stored in rows R0, R1, R2 and R3 of register file 301 are transferred to rows R0, R8, R16 and R24, respectively, of RAM 200. This process requires four 4-bit read operations from register file 301 and four 4-bit write operations to RAM 200. The four write operations to RAM 200 are staggered by eight rows, thereby promoting the separation of consecutive data bits within the interleaved data stream. (Boner col. 6, lines 39-46).

On the contrary, in the present application a method to implement a column interleaving function is disclosed where in a first step a number of separate memories are provided equal to the maximum number of columns in the interleaver function. This is explained in the application in par. [0024] (see p.4, l.22-23) and in par. [0025] (see p.5, l.4). As stated in par. [0023], using distributed memory offers an advantage in terms of power consumption.

An exemplary embodiment of the claimed feature of providing a number of memories equal to the maximum number of columns in the interleaving function is shown by bit RAMs 1

through 8 in FIG. 3 of the present application:

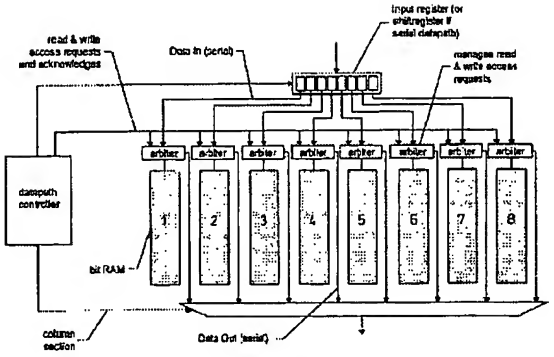

Fig. 3

Boner utilizes a single RAM memory 200 and diverts as much use as possible from the RAM memory to the register 301 to avoid power consumption:

> Significantly, register file 301 consumes much less power than full-size RAM 200. This is because register file 301 has relatively short bit and word lines, which have relatively small capacitances. Because register file 301 has shorter bit lines than RAM 200, register file 301 does not need to implement sensitive sense amplifiers, thereby resulting in further power savings. In the described embodiment, register file 301 consumes about one to two times less power than RAM 200 for a similar operation. In addition to the power savings, the smaller size of register file 301 enables register file 301 to operate faster then RAM 200. In the described embodiments, register file 301 is one to two orders of magnitude faster than RAM 200. (Boner col. 5, lines 55-67).

Moreover, to expand the memory capacity of the Boner device, the size of the single RAM memory is increased or additional register files are added but more than one RAM is not used in accordance with the intent to reduce power consumption:

> The present invention, as exemplified above, can be expanded in several ways. For example, although block interleaver 300 has been described in connection with a 4x32 RAM and a 4x4 register file, these elements can have different sizes (both in the number of columns and the number of rows) in other embodiments. For example, block interleaver 300 can be modified to have an 8x8 register file and an 8x2500 RAM. A block

> interleaver of this size is capable of operating in accordance with the proposed 3GPP standard. . . . In another embodiment, register file 301 can be implemented using two or more register files working in parallel. In such an embodiment, while a first set of data values is written into one register file, a second set of data values is transferred from another register file into RAM 200. Boner col. 7, lines 63 through col. 8, line 48).

The Office Action asserts that Boner discloses a number of columns equal to the length of each incoming data bit. The Office Action further asserts that this is the equivalent of utilizing a number of memories equal to the maximum number of columns in the interleaving function. Applicant respectfully disagrees. A single RAM having multiple columns is clearly different in structure and function from a number of memories equal to the maximum number of columns in the interleaving function as in claims 16 through 30. For example, in the present invention utilizing a distributed memory approach, a read operation only activates the memory containing the data element to be read and thus there is no power wasted on activating the other memories.

Additionally, claim 17 of the present application includes the feature of the data entities in the input stream being first written into a register and when the register is filled, the step of writing into a memory is applied. It is respectfully submitted that this feature cannot be found in Boner. In Boner, data is first written into a (small) register file, and then transferred from the register file to the actual interleaver memory. Table 3 and Table 4 in Boner, column 7, illustrate the actual operations for a 32x4 example:

The operation of block interleaver **300** will now be compared with the operation of interleaver RAM **100**. Table 3 summarizes the operations performed by interleaver RAM **100** in order to create a 128-bit interleaved data stream.

TABLE 3

Write Operations	Read Operations
32 4-bit write operations to interleaver RAM 100	128 4-bit read operations from interleaver RAM 100

Table 4 summarizes the operations performed by block interleaver **300** in order to create the same 128-bit interleaved data stream as interleaver RAM **100**.

TABLE 4

Write Operations	Read Operations
32 4-bit write operations to register file 303 32 4-bit write operations to RAM 200	32 4-bit read operations from register file 303 32 4-bit read operations from RAM 200

Additionally, claims 16 through 28 include the feature of performing selection and permutation on the memories, e.g., at the distributed memory level. In contrast, the Boner permutation (interleaving function) is executed at the register file, prior to writing to the single RAM memory.

The Office Action rejects claims 11 and 15 under 35 U.S.C. §103 as being obvious over Boner in view of U.S. Patent No. 4,672,605 to Hustig. This rejection is moot as to claims 11 and 15, which have been cancelled.

With respect to claims 16 through 30, as described above, Boner fails to disclose or suggest the feature of these claims of providing a number of memories equal to the maximum number of columns in the interleaving function. Similarly, Hustig fails to disclose or suggest this feature. Hustig discloses the use of a single RAM in its interleaver:

> The random access memory 74, two multiplexer chips, 76, 78, and a main program counter 82 constitute the main elements of the bit interleaver 85 which is timed off the main clock crystal. The program counter or sequence generator, 82, is connected to the multiplexers, 76, 78, so that addresses are supplied to the RAM, 74, in the proper format. A first sequence of addresses is provided to write the data into bit locations in serial order by column, as illustrated in FIG. 3. A second read sequence is provided to supply the correct addresses to read the data bits out serially by rows, as

> also illustrated in FIG. 3. It will be understood that the rows can be sequentially read out in any order. (Hustig col. 5, lines 3-15).

Thus, the combination of Boner and Hustig do not disclose or suggest the feature of claims 16 through 30 of providing a number of memories equal to the maximum number of columns in the interleaving function. Given the above-mentioned differences between the present invention and the disclosure of Boner, it is clear that the skilled person would never arrive at the invention by combining the teachings of Boner and Hustig.

Moreover, there is a lot more to say about the drawbacks of the Boner approach. The register file approach is different from the shift register approach in that it is less flexible, and involves in total more memory accesses. The Boner approach is also not practical if the interleaver dimensions become somewhat bigger. In 3GPP (W-CDMA), schemes of the order of magnitude of 20x250 are applied. In future schemes, the largest dimensions might be leading to tables with up to 40,000 elements. In those cases, the register file power consumption as in Boner will be very significant. The solution according to the present invention does not suffer from this drawback.

It should also be noted that in Boner's approach, the 4-bit write operations to the register file must be preceded by some mechanism to organize the input bits in 4-bit chunks. This is not disclosed in Boner. In the present application, it is clearly indicated how to remove bottlenecks with data at the input. Concerning the read operation, the solution according to the invention is power efficient and flexible. The read operation only activates the memory containing the data element to be read; no power is wasted on activating the other memories (distributed memory approach). It is more flexible as there is more freedom concerning the permutation scheme.

In claim 19 the feature is disclosed of data entities being multiple bit words. Boner's method is not applicable to multiple-bit words, as his register file + single RAM concept cannot accept multiple-bit words. However, the extension to multiple-bit words is important in receiver architectures involving soft decoding. This is the case in most current and future air interface schemes for high-speed data streaming or communication.

In view of the above, applicant respectfully urges that the objection be reconsidered and withdrawn, and that this application be passed to allowance.

Sincerely,

6/1/06
Date

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